

REMARKS

The Examiner is respectfully requested to enter the amendment to claim 21 after final rejection to correct a typographical error, thereby rendering the claim in better form for appeal should the Examiner continue to reject claims in view of the cited prior art.

Claims 21-24 and 29-30 are finally rejected under 35 U.S.C. 102(b) as being anticipated by U.S. patent 5,569,952 (HAYASHI). The applicant respectfully requests the Examiner to withdraw the rejection of these claims for the reasons indicated below.

Claim 21

The applicant's invention recites (as illustrated by FIG. 4) an electronic system including a "base die" 82, a "secondary die" 86, a substrate 98, and some conductive contacts 92 extending between the base die and the substrate. The secondary die (84) is recited as residing between the base die 82 and the substrate 98, and as being directly connected through signal paths 81 to base die 82.

HAYASHI shows in FIGS. 1 and 3 a set of "electronic devices" 3 residing on a printed circuit board (PCB) 2 to form a hybrid circuit 1. FIG. 3 shows the PCB 2 of hybrid circuit 1 as being connected to another PCB 5 via signal paths 6. Thus in FIG. 3 we see an "electronic device" 3 residing between two PCBs 1 and 5, with the electronic device 3 being connected by signal paths to PCB 1 and with PCB 1 being connected by signal paths 4 to PCB 5.

The applicant remains confused as to the Examiner's position as to which elements of HAYASHI anticipate each element of claim 21. The Examiner's initial position as indicated on page 2 of the office action (we will call it "position A"), is that HAYASHI anticipates claim 21 because

- a. PCB 2 is the recited "base die",
- b. Hybrid IC 1 is the recited "substrate",
- c. electronic element 3 is the recited "first secondary die", and
- d. terminals 4 are the recited "conductive contacts".

Since both the Examiner and HAYASHI consider PCB 2 to be a part of hybrid circuit 1, position A is somewhat ambiguous as to whether the Examiner considers PCB 2 to be the "base die" or part of the "substrate".

At the top of page 3 of the office action, the Examiner again asserts that the PCB 2 is the "base die" but now asserts that PCB 5 of FIG. 3, rather than hybrid circuit 1, is the "substrate". Thus the Examiner's position ("position B") appears to be as follows:

- a. PCB 2 is the recited "base die",
- b. PCB 5 is the recited "substrate",

- c. electronic elements 3 are the recited "first secondary die, and
- d. terminals 4 are the recited "conductive contacts.

Another statement on page 3 of the office action ("the hybrid IC body (1) can be considered as a base IC die") casts some doubt on whether either of positions A or B is the Examiner's true position since it seems to indicate that the Examiner considers hybrid IC 1, rather than PCB 2 to be the "base die". Perhaps the Examiner's true position (position C) is as follows:

- a. Hybrid IC 1 is the recited "base die",
- b. PCB 5 is the recited "substrate",
- c. electronic elements 3 are the recited "first secondary die, and
- d. terminals 4 are the recited "conductive contacts.

The Examiner's comments on page 4 of the office action lend support to position B; however the applicant will respond to all three of the examiner's positions.

1. The Examiner's position A that the applicant's recited "substrate" (claim 21) reads on hybrid IC 1 is correct at least to the extent that hybrid IC 1 does include a PCB 2 which is a type of substrate. The Examiner's position B or C that the applicant's recited "substrate" reads on PCB 5 is also correct insofar as PCB 5 includes a substrate.

2. The Examiner's positions A, B and C that the applicants' recited "secondary IC die" reads on HAYASHI's "electronic elements 3" is not correct. The Examiner states that:

"The electronic component (3) typically is integrated circuit chips or IC chips which is consider as IC dies (or other terminology term)".

HAYASHI calls items 3 "electronic elements" but provides no indication as to what kind of electronic elements they may or may not be. To some extent HAYASHI teaches away from devices 3 being IC dice. As illustrated in FIGs. 1 and 2, electronic elements 3 do not look like an IC die because each has what appears to be conductors extending outward from its edges. IC dice are linked to the external circuits though conductors extending from their surfaces and not from their edges. See for example the applicant's FIG. 4 where IC dice 84-86 communicate via solder ball conductors on their upper surfaces. Moreover, since claim 21 is rejected under 35 USC 102, the Examiner must show that HAYASHI directly teaches that at least one electronic competent 3 is an

IC die; the Examiner's suppositions as to what electronic elements "typically" consist of are irrelevant.

3. The Examiner's position A, B or C that PCB 2 or hybrid circuit 1 is the recited "base IC die" is incorrect. The Examiner seems to suggest that "IC die", a "hybrid circuit" and a "printed circuit board" (PCB) are all the same thing, however those of skill in the electronic arts consider these to be three distinctly different things. To help the Examiner distinguish between an IC die, a hybrid circuit and a PCB, each term is separately discussed below.

An "IC die", also called an integrated circuit chip, is a small piece of semiconductor material doped to form electronic devices therein and includes conductors formed on insulating layers above the semiconductor material interconnecting the devices formed within the semiconductor material so that they form an integrated circuit. The on-line ecommerce-guide.com dictionary of electronics terms (<http://e-comm.webopedia.com/TERM>) defines a die as "[A] square of silicon that contains an integrated circuit." The on-line Glossary of Printed Circuit Design and Manufacturing (<http://www.goldengategraphics.com>) published August 26, 2002 by Golden Gate Graphics, a company in the business of designing printed circuit boards, defines a "die" as "an integrated circuit manufactured on a semiconductor substrate and then cut or etched away from the silicon wafer." Of course not all IC die are formed on silicon, as other semiconductor materials such as germanium are sometimes used.

A "PCB" is a board upon which electronic devices such as ICs and other components can be mounted. A PCB usually comprises one or more layers of insulating material along with conductive traces formed on and passing through the insulating layers for interconnecting the devices to be mounted on the PCB. The Glossary of Printed Circuit Design and Manufacturing defines a printed circuit board as a "flat plate or base of insulating material containing a pattern of conducting material. It becomes an electrical circuit when components are attached and soldered to it."

A "hybrid circuit" is an electronic circuit formed by two or more different kinds of discrete electronic devices such as ICs, resistors, capacitors etc. The Glossary of Printed Circuit Design and Manufacturing defines a "hybrid circuit" as "[a]ny circuit made by using a combination of the following component manufacturing technologies: monolithic IC, thin film, thick film and discrete components." Note that since HAYASHI indicates that hybrid circuit 1 is formed by a PCB 2 and a plurality of "electronic devices"

3, HAYASHI's use of the term hybrid circuit is not in-consistent with its generally accepted definition.

From the above discussion, it should be apparent that a PCB is not an IC die because unlike an IC die, a PCB is not formed of semiconductor material containing an integrated circuit. Also it should be understood that an IC die is not a hybrid circuit because unlike a hybrid circuit, an IC die is a circuit formed by only one discrete component (a chip) whereas a hybrid circuit is formed by more than one discrete component. Thus those of ordinary skill in the electronics arts do not consider "IC die", "PCB", and "hybrid circuit" to be synonyms; they are different things. Claim 21 is therefore patentable over HAYASHI because HAYASHI does not disclose the recited "base IC die". Neither the hybrid IC 1 nor PCB 2 can be considered a "base IC die" since neither is an IC die. Not does HAYASHI disclose one "secondary die" residing between another "base die" and a PCB as recited in claim 21. HAYASHI discloses only an electronic element 3 (which is not described as being an IC die) residing between two PCBs 2 and 5.

4. The Examiner's positions A, B and C that the recited "conductive contacts" of claim 21 reads on terminals 4 of HAYASHI's FIG 4 is incorrect. Claim 21 recites that the conductive contacts are "for conveying signals between the base IC and the conductors on the substrate." HAYASHI teaches that terminals 4 are designed to convey signals between two PCBs and provides no indication that contacts 4 could be used as conductive contacts for connecting a die to a PCB as recited in claim 21.

The applicant's invention of claim 21 can be considered an improvement to HAYASHI in that instead of mounted electronic circuits 3 on a PCB so that they have to communicate with one another through traces on the PCB, the applicant directly links a secondary die containing an integrated circuit to a base die which also contains an integrated circuit. Thus the ICs in the applicant's secondary and base die can directly communicate with one another without having to transmit signals to one another via traces on a PCB. Claim 21 is therefore patentable over HAYASHI.

Claims 22-31

Claims 22-24 and 29-30 depend on claim 21 and are patentable over HAYASHI for similar reasons.

Claim 22 is additionally patentable over HAYASHI because HAYASHI fails to disclose solder forming the first conductive signal paths between a base IC die and a secondary IC die as recited in claim 22. The Examiner cites HAYASHI column 4, line 49 as disclosing solder forming paths between two IC dice. However this section of HAYASHI mentions only that solder connects a terminal

4 to electrodes on a PCB 2. There is no suggestion of using solder to provide paths between two IC dice.

Claim 24 is additionally patentable over HAYASHI because it recites that the substrate of claim 1 is a "semiconductor substrate". The Examiner supposes without justification that PCB 5 of FIG. 3 is a semiconductor substrate and does not point to any portion of HAYASHI that makes that assertion. Nothing in HAYASHI indicates that PCB 5 is a semiconductor substrate or anything other than a PCB, and PCBs are not formed of semiconductor material.

Claims 29 and 30 are additionally patentable over HAYASHI because they recite a second secondary IC die and second conductive paths between the secondary IC and a second surface of the base IC die. Claim 29 reads, for example, on the applicant's FIG. 11 where first and secondary die 214 and 221 connected through signal paths 227 and 218 to both the upper and lower surfaces of base die 212. HAYASHI does not disclose any such structure.

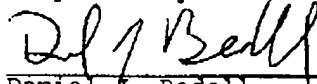
Claim 30 further recites vias providing signal paths between the first and second surfaces of the base IC die. See for example vias 224 of the applicant's FIG. 11. HAYASHI teaches no such vias in an IC die.

Claims 25-28 and 30-31 are finally rejected under 35 USC 103(a) as being unpatentable over HAYASHI in view of U. S. Patent 6,330,164 (KHANDROS).

Claims 25-28 and 30-31 depend on claim 21. The Examiner cites HAYASHI as disclosing subject matter of parent claim 21 and cites KHANDROS as teaching the additional subject matter set forth in claims 25-28 and 30-31. The comments above distinguishing claim 21 over HAYASHI are applicable to claims 25-28 and 30-31 and the applicant stands by the comments made in the previous office action distinguishing claims 25-28 and 30-31 over the combination of HAYASHI and KHANDROS. Neither HAYASHI nor KHANDROS teach or suggest a secondary IC die connected to a base IC die, such that the secondary IC die resides between the base IC die and a substrate.

It is believed that in view of the foregoing amendments and remarks, the application is in condition for allowance. Notice of Allowance is therefore respectfully requested.

Respectfully submitted,



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